

FPGA 1 Specification

64 port G-PON

ASGvOLT64

(GPON OLT)

Version: 1.0

Revision History

Document Rev.	Date	Author	Revision Description	CPLD code version
1.0	8/29/2019		Initial OCP release	

3.1. Offset 0x01 FPGA version (Read Only)

Example : version 5.01 then reg 0x1 is 5, reg 0x2 is 1

Bit	Name	R/W	Reset Value	Description
7:0	FPGA_ver[7:0]	R		FPGA version

3.2. Offset 0x02 FPGA version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FPGA_ver[7:0]	R		FPGA version

4.1. Offset 0x01 System Reset_1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	Reserved			
3	P1014A_3_reset	R/W	1	1: Normal status 0: Reset P1014A_3 by SW.
2	P1014A_2_reset	R/W	1	1: Normal status 0: Reset P1014A_2 by SW.
1	P1014A_1_reset	R/W	1	1: Normal status 0: Reset P1014A_1 by SW.
0	P1220A_RESET	R/W	1	1: Normal status 0: Reset P1220A by SW.

4.2. Offset 0x02 System Reset (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	Reserved			
0	Module_RST_L	R/W	1	1: Normal status. 0: Reset PHY by SW.